



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s): Osann, Jr., et al.
Appl. No.: 09/827,015
Confirm. No.: 3460
Filed: April 5, 2001
Title: DEPOPULATED PROGRAMMABLE
LOGIC ARRAY

PATENT APPLICATION

Art Unit: 2816
Examiner: L. Nguyen

Customer No. 23910

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Larry T. Harris, Reg. No. 44,745
Signature Date: October 16, 2002

RESPONSE TO OFFICE ACTION UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, DC 20231

Sir:

Remarks

These Remarks are in reply to the Office Action mailed July 16, 2002.

Claims 1-50 were pending in the Application prior to the outstanding Office Action. In the current Office Action, the Examiner has indicated that Claims 1-50 are subject to restriction in accordance with one of the following two groups:

- I. Claims 1-23 and 49-50, drawn to a method or process for forming a programmable logic array (PLA), which can be implemented manually and/or with a computer, classified in class 716, subclass 16; and
- II. Claims 24-48, drawn to a structure of an integrated circuit with a PLA therein, classified in class 326, subclass 39.

Applicant elects to pursue the claims of Group II, Claims 24-48, and withdraws the non-elected claims.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 06-1325 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: October 16, 2002

By: 

Larry T. Harris
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